Remarks

In the Final Office Action dated November 27, 2009, the drawings are objected to, and the following new grounds of rejection are presented: claims 1-14 stand rejected under 35 U.S.C. § 103(a) over Yamada (U.S. Patent No. 5,757,639) in view of Stancil (U.S. Patent No. 6,272,584) and May (U.S. Patent No. 7,343,483); and claims 15-18 stand rejected under 35 U.S.C. § 103(a) over the '639 reference in view of the '584 reference and further in view of Chang (U.S. Patent No. 6,484,273). In the following discussion, Applicant does not acquiesce in any regard to averments in this Office Action (unless Applicant expressly indicates otherwise).

Applicant respectfully traverses the § 103(a) rejections of claims 1-9 because the cited combination of references lacks correspondence. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including, *e.g.,* aspects of the claimed invention directed to coupling of the plurality of integrated ICs to one another through test circuitry. Applicant is uncertain how the asserted first and second ICs of reference '483 are coupled through test circuitry. The Office Action cites PLD Controller 240 of Figure 2 of the '483 reference as the claimed test circuitry. The only support for this asserted conclusion is an input port to the PLD controller 240 with a label "PLD test Interface." There is no description of this port or any test functionality provided elsewhere in the '483 reference. Having one port listed as a test interface, one reasonable interpretation is that PLD controller 240 includes some test circuitry for the testing of the PLD controller 240. However, this reasoning does not extend to the erroneous conclusion that all paths through the PLD controller pass through test circuitry. If such were the case, any circuit having an externally accessible JTAG port would constitute testing circuitry regardless of actual function. Without further description, one skilled in the art could also reasonably conclude that the described port of PLD controller 240 is connected to an external "PLD test Interface," and the PLD controller includes no test circuitry. Applicant submits that the Office Action has not presented a convincing line of reasoning why a skilled artisan would understand that the '483 reference explicitly or implicitly suggests that first and second ICs of the '483 reference are coupled through test circuitry. *See* M.P.E.P §706.02(j). Because the Office Action has not particularly shown support or provided reasoning for the conclusion that the PLD controller 240

constitutes test circuitry, a *prima facie* case of obviousness has not been made and the rejections cannot stand.

Applicant respectfully traverses the § 103(a) rejections of claims 10-14 for similar reasons as that of claims 1-9. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including, *e.g.,* aspects of the claimed invention directed to transmitting using debugging circuitry. As stated above, the Office Action has not particularly shown support or provided reasoning for the conclusion that the portion of the cited PLD controller 240 of Figure 2 of the '483 reference used for communication between first and second ICs constitutes debugging circuitry. Therefore, a *prima facie* case of obviousness has not been made and the rejections cannot stand.

Applicant further traverses the 103 rejection of claim 4 because the cited combination of references lacks correspondence. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including, *e.g.,* aspects of the claimed invention directed to executing at least a portion of the first set of programming instructions prior to transmitting the second set of programming instructions to the second IC. Applicant submits that Figure 6 of the '639 reference cited in the Office Action does not disclose the execution of the first set of programming instructions prior to transmission of the second set of instructions to the second IC. In contrast, Figure 6 clearly shows that the first set of instructions stored in the first IC (element S3 of Figure 6) is executed (element S6 of Figure 6) after transmitting the second set of instructions to the second IC (element S5 of Figure 6). *See also* Col. 2:50 through Col. 3:3 of the '639 reference. Because the asserted '639 reference does not disclose the aspects of the present invention as asserted in the Office Action, no reasonable interpretation of the asserted prior art, taken alone or in combination, provides correspondence. As such, a proper §103 rejection has not been presented and Applicant requests that the rejection be withdrawn.

Applicant further traverses the §103(a) rejections of claims 6 and 10-14 because the '639 reference, either alone or in combination with the '483 and '584 references, lacks correspondence. None of the asserted references appears to relate to the claimed invention when viewed "as a whole" (§ 103(a)) including aspects regarding first and second test circuits corresponding to first and second ICs. The Office Action acknowledges that the '639 and '584 references fail to disclose the aspects regarding test

circuitry. *See* pages 3, 7, and 10 of the Office Action. Application of the '483 reference fails to cure these deficiencies. Regarding claim 6, it is unclear how the cited Figure 2 of the '483 reference is interpreted as disclosing test circuitry of each of the ICs having a test input for a test mode signal. The Office Action has not particularly pointed out respective inputs for a test mode signal corresponding to the first and second ICs. Rather, the Office Action cites to only one input (PLD test interface of Figure 2). Further, the cited Figure 2 does not illustrate a data flow in which a test input received at the asserted input port would be forwarded to each of the first and second circuits. Nor has the Office Action asserted and provided reasoning that this functionality is either implicit or inherent. Regarding claims 10-14, for similar reasoning to that stated above, it is unclear how the cited Figure 2 of the '483 reference is interpreted as disclosing first and second ICs each having test circuitry for providing debugging functionality. Because the references fail to disclose these operable aspects, no reasonable combination of the references would provide correspondence for claims 6 or 10-14. As such, the § 103 rejections fail and Applicant requests that they be withdrawn.

Applicant further traverses the §103(a) rejection of claims 15-18 because the '639 reference either alone or in combination with the '273 and '584 references lacks correspondence. None of the asserted references alone or in combination appears to relate to the claimed invention when viewed "as a whole" (§ 103(a)) including aspects regarding first and second test circuits, each test circuit configured and arranged to communicate debugging information in a test mode and communicate code images in another mode. The '273 reference does not appear to disclose a test circuit that communicates debugging information in a test mode and communicates code images in another mode as asserted in the Office Action. In contrast the portions of the '273 reference cited in support of the rejection only disclose JTAG circuitry configured to communicate test data. Similar to the rejections of claims 1-9, the rejections of claims 15-18 appear to rely on the erroneous conclusion that the entire circuit shown in the cited Figure 2 of the '273 reference constitutes test circuitry merely because a JTAG module is provided in one portion of the circuit. Applicant submits that such an interpretation is contrary to the plain meaning of the claimed aspects of the invention.

Further, the Office Action has not provided any motivation to arrange test circuits in each IC to communicate code images while in a non-testing mode. Applicant submits

that the Examiner has simply identified JTAG circuitry as common circuit elements (which can be found in any number of references) and then arranged these elements, using the claimed invention as a template, to provide testing circuitry arranged to communicate code images while in a non-testing mode. This is the hallmark of improper hindsight reconstruction with the proposed combination being derived, not "on the basis of the facts gleaned from the prior art," but solely from Applicant's disclosure. *See, e.g.,* M.P.E.P. § 2142. As explained in M.P.E.P. § 2143, "(t)he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." As JTAG circuitry is not taught to be used in the manner claimed nor is there any suggestion toward this end in the references, the rejection cannot stand and there is not a *prima facie* case of obviousness.

In response to the objection to the drawings, Applicant submits that the objection is improper and not required under 37 C.F.R. 1.83(a). In support of Applicant's position reference is made to 35 USC §113 and M.P.E.P. § 601.01(f), which indicate that "applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented." The Office Action has not indicated why one skilled in the art would not be able to understand the claimed invention. In addition, M.P.E.P. § 601.01(f) indicates that it has been PTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 USC §113. Since most of the claims in the current application are method claims, Applicant has complied with M.P.E.P. § 601.01(f).

Notwithstanding M.P.E.P. § 601.01(f), Applicant submits that the claimed feature is adequately described by the reference to the numerical labels shown in Figures 4-8. For example, the description of Figure 7 at paragraph 0043 of Applicant's published application describes, with reference to the numerically labeled elements:

> In a first operation 702, a first program code is transferred from a first memory to a first integrated circuit. . . .The first program code is stored 704 in the first IC. . . a second program code is transferred 706 from the first memory to the first IC, and the second program code is transmitted 708 from the first IC to a second IC that is coupled to the first IC. . . . The second program code is stored 710 in the second IC.

Notwithstanding the above, for the purpose of facilitating prosecution of the current application, Applicant has submitted replacement drawings of Figures 4-8 as suggested by the Examiner.

In view of the above, Applicant believes that each of the rejections is improper and should be withdrawn and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170 (or the undersigned).

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Attachment: Replacement Drawings—Five Sheets